IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Japanese Unexamined Patent Application Publication of
Takashi Nihonmatsu et al.
Japanese Unexamined Patent Application Publication Number: JP2002-203823
Publication Date: July 19, 2002
For: METHOD FOR PROCESSING SEMICONDUCTOR WAFER AND SEMICONDUCTOR WAFER

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March 4, 2010 Masayoshi Suda

Date Masayoshi Suda

(19) Japan Patent Office (JP)

(12) Unexamined Patent Publication Bulletin (A)

(11) Patent Application Laid-open Disclosure Number: Japanese Patent Application Laid-open No. 2002-203823 (P2002-203823A)

(43) Laid-open Disclosure Date: July 19, 2002 (2002.7.19)

(51) Int.CL.[7]	Domestic Classification Symbol	FI	Theme Code (reference)
H01L 21/304	622	H01L 21/304	622N 5F043
21/02		21/02	B
21/306		21/308	B
21/308		21/306	B

Examination Request: Unrequested

Number of Claims: 16

OL (19 pages in total)

(21) Application Number: Japanese Patent Application No. 2001-179779 (P2001-179179)

(22) Application Date: June 13, 2001 (2001.6.13)

(31) Priority Application Number: Japanese Patent Application No. 2000-196946 (P2000-196946)

(32) Priority Date: June 29, 2000 (2000.6.29)

(33) Priority Country: Japan (JP)

(31) Priority Application Number: Japanese Patent Application No. 2000-333480 (P2000-333480)

(32) Priority Date: October 31, 2000 (2000.10.31)

(33) Priority Country: Japan (JP)

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(54) [Title of the Invention] METHOD FOR PROCESSING SEMICONDUCTOR WAFER AND SEMICONDUCTOR WAFER

(57) [Abstract]

[Problem to be Solved] To provide a method for processing a semiconductor wafer, which improves a flatness degree and surface roughness of the wafer and a state of a wafer back side.

[Solution] This method for processing the semiconductor wafer, wherein a chambering step, a lapping step, an etching step, and a mirror polishing step are performed, is characterized in that, in the etching step, acid etching is performed after alkali etching, in which acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water. Further, a method for processing the semiconductor wafer comprising the steps of chamfering, surface grinding, etching, and mirror polishing is characterized in that the etching step is performed as above. Further, a method for processing the semiconductor wafer, wherein a flattening step, an etching step, and a mirror polishing step are performed, is characterized in that the etching step is performed as above and, in the mirror polishing step, a back surface polishing step is performed after the acid etching, and then a front surface polishing step is performed.

[Type of Document] Claim(s)

[Claim 1]

A method for processing a semiconductor wafer, the method effecting at least a chamfering step, a lapping step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, wherein acid etching is performed after alkali etching at the etching step, and the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step.

[Claim 2]

A method for processing a semiconductor wafer, the method effecting at least a chamfering step, a surface grinding step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, wherein the surface grinding step is performed before the etching step, acid etching is performed after alkali etching at the etching step, and the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step.

[Claim 3]

The method for processing a semiconductor wafer according to claim 2, wherein a lapping step is added to the method for processing the semiconductor wafer, and processing is performed in the order of the lapping step,

the surface grinding step, and the etching step.

[Claim 4]

A method for processing a semiconductor wafer, the method effecting at least a flattening step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, wherein the flattening step is performed before the etching step, acid etching is performed after alkali etching at the etching step, the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step, a back surface polishing step is carried out and then a front surface polishing step is performed at the mirror polishing step after the acid etching.

[Claim 5]

The method for processing a semiconductor wafer according to claim 4, wherein the flattening step is a lapping step and/or a surface grinding step.

[Claim 6]

The method for processing a semiconductor wafer according to claim 4 or 5, wherein, at the back surface polishing step, polishing is carried out in such a manner that a gloss level of 35 to 50% can be obtained.

[Claim 7]

The method for processing a semiconductor wafer according to claims 2, 3, 5, and 6, wherein grinding is

performed at the surface grinding step so as to increase a thickness of a wafer outer peripheral portion.

[Claim 8]

The method for processing a semiconductor wafer according to any one of claims 1 to 7, wherein an entire etching removal in the etching step is 30 μm or below on both surfaces.

[Claim 9]

The method for processing a semiconductor wafer according to any one of claims 1 to 8, wherein a polishing stock removal in the mirror polishing step is 7 μm or below.

[Claim 10]

The method for processing a semiconductor wafer according to any one of claims 1 to 9, wherein, as a composition ratio when blending the acid etchant, a hydrofluoric acid concentration is 5 to 15 weigh% and a phosphoric acid concentration is 10 to 40 weight%.

[Claim 11]

The method for processing a semiconductor wafer according to any one of claims 1 to 10, wherein the acid etchant is obtained by dissolving silicon with a concentration of 10 g/L or above.

[Claim 12]

The method for processing a semiconductor wafer according to any one of claims 1 to 11, wherein, as a composition ratio when using the acid etchant, a

hydrofluoric acid concentration is 1 to 7 weight% and a phosphoric acid concentration is 18 to 33 weight%.

[Claim 13]

The method for processing a semiconductor wafer according to one of claims 1 to 12, wherein an alkali etchant of the alkali etching is one of an NaOH aqueous solution and a KOH aqueous solution.

[Claim 14]

A semiconductor wafer processed by the method set forth in any one of claims 1 to 13.

[Claim 15]

A semiconductor wafer subjected to chemical etching, wherein a maximum value of a pit depth is equal to or below 4 μm, waviness is equal to or below 0.05 μm, and a gloss level is 20 to 70%.

[Claim 16]

A semiconductor wafer having a surface subjected to mirror polishing, wherein SFQRmax is equal to or below 0.1 μm, and the other surface subjected to mirror polishing has a pit depth maximum value of 4 μm or below, waviness of 0.05 μm or below, and a gloss level of 20 to 70%.

[Detailed Description of the Invention]

[0001]

[Technical Field Pertinent to the Invention]

The present invention relates to an improvement in a method for using chemical etching to remove a

mechanically damaged layer on a wafer surface produced in a manufacturing process of a semiconductor wafer, especially a single-crystal silicon wafer and an improvement in a wafer back surface state produced in a method for manufacturing a single-crystal silicon wafer.

[0002]

[Background Art]

In conventional technologies, a semiconductor mirror finished wafer manufacturing process usually includes a step of slicing a single-crystal rod of silicon or the like and steps of effecting at least chamfering, lapping, etching, mirror polishing, and cleaning/drying the obtained semiconductor wafer. FIG. 3 shows an example of manufacturing steps of such a semiconductor mirror finished semiconductor wafer. In these steps, some of the steps may be counterchanged or repeated for a plurality of number of times, or other steps such as a heat treatment or grinding may be added or replaced to carry out various processes depending on a purpose. For example, a grinding step is carried out on three stages, or a surface grinding step is added before a polishing step in some cases.

[0003]

Usually, etching is performed for the purpose of removing a mechanically damaged layer on a surface that is introduced at the time of machining such as slicing, chamfering, or lapping, and the etching step is carried

out after a flattening step such as a lapping step. For example, an acid etching step of etching a wafer surface for several to several-ten μm is usually effected by using a mixed acid aqueous solution containing a hydrofluoric acid, a nitric acid, an acetic acid, and water.

[0004]

According to the acid etching, although the mechanically damaged layer is removed, a flatness degree of a wafer is apt to be jeopardized when an etching removal is large. In particular, a peripheral portion of a wafer has a larger etching amount than other portions, and a flatness degree of this portion is considerably degraded. Further, there is also a problem that harmful NO_x is generated due to a chemical reaction at the time of acid etching, for example.

[0005]

To avoid these problems, alkali etching is used in some cases. However, when an alkali-based etching solution is used as an etchant to perform etching, a flatness degree after lapping is maintained as it is, but a pit having a depth of several μm and a size of several to ten-odd μm is apt to be locally formed on a wafer surface. It is considered that a portion having a large local mechanical damage produced at a lapping step is deeply etched due to anisotropy of alkali etching as compared with other portions, thereby forming the pit.

[0006]

As described above, the flatness degree of the wafer is degraded due to etching when acid etching is carried out, the deep pit is formed when alkali etching is effected, and hence a polishing stock removal of mirror polishing must be increased to remove these problems. However, when the polishing stock removal is increased, the flatness degree may be degraded by polishing, and productivity of the polishing step is greatly lowered.

[0007]

Thus, as disclosed in Japanese Patent Application Laid-open No. 1999-233485, the present application tried solving the problems by performing acid etching after alkali etching at an etching step and increasing an etching removal of the alkali etching to be larger than an etching removal of the acid etching using a mixed acid aqueous solution containing a hydrofluoric acid, a nitric acid, an acetic acid, and water, whereby sufficient flatness was achieved, but a reduction in polishing stock removal for obtaining a mirror polished wafer (a polished wafer, PW) was not necessarily sufficient. In recent years, realization of a higher flatness degree is demanded, decreasing a polishing stock removal is more important.

[0008]

Therefore, a technology that reduces a polishing

time or avoids outer periphery sag by performing a (surface) grinding step immediately before a polishing step and then polishing a wafer surface was considered. However, grinding striations due to grinding remain, or controlling a grinding damage is difficult, and suppressing the grinding damage to 3 μm or below is difficult.

[0009]

Furthermore, it was revealed that a reduction in wafer back surface brightness (a gloss level) and waviness (surface roughness in cycles of 2 mm or above) occur and contamination called blue stain (which may be simply referred to as stain hereinafter) which is readily produced in a low-resistivity crystal is apt to be generated. In particular, the gloss level of the wafer back surface may be reduced approximately 15 to 20% depending on conditions of an etching step (e.g., when an etching removal is reduced) in particular.

[0010]

It is to be noted that the gloss level of a wafer (a back surface) in the present invention was measured by making reference to JIS Z 8741 (a specular gloss measuring method) and using a specular glossmeter (a glossmeter SD) specified in this standard based on a method conforming to the same. That is, assuming that brightness in a state where nothing is placed at an object position is determined as 0% for the convenience

sake, and evaluation was carried out under setting conditions that a gloss level of a mirror finished wafer is determined as 100%.

[0011]

Although both front and back surfaces of a wafer are subjected to mirror polishing in some cases in conventional examples, when the back surface is determined as a perfect mirror finished surface (when a gloss level is set to approximately 100%), there are problems such as easy attachment and detachment of particles, a contact area of an electrostatic chuck or the like that adsorbs the wafer, and others, and the gloss level must be reduced to a certain range. Although depending on a device process and others, a gloss level of approximately 30 to 60% is generally preferable.

[0012]

Usually, the gloss level on the wafer back surface is mainly determined at the etching step. To obtain a wafer having a high flatness degree, reducing an etching removal at the etching step is preferable. In the method for performing the acid etching after the alkali etching, it is preferable to perform etching with an etching removal in the alkali etching being set to 10 to 30 μm, especially 20 μm for both surfaces and an etching removal in the acid etching being set to 5 to 20 μm, especially approximately 10 μm for both the surfaces,

and an etching removal in the entire etching process is approximately 30 to 40 μm for both the surfaces. As a result, the gloss level can be adjusted to approximately 40%, but the gloss level is lowered to become 20% or below when the etching removal is to be further reduced, thus resulting in a problem. Therefore, when the method for processing a semiconductor wafer by which the acid etching is carried out after the alkali etching is adopted, a quality of a back surface side may become a problem in particular.

[0013]

[Problem to be Solved by the Invention]

In view of the above-described problem, it is, therefore, an object of the present invention to provide a method for processing a semiconductor wafer that can remove a mechanically damaged layer while maintaining a flatness degree of a wafer, improve surface roughness, reduce depths of local deep pits in particular, fabricate a chemical etched wafer (CW) which has a smooth irregular shape and an etched surface that particles or contamination is hardly produced, reduce a polishing stock removal in a mirror polishing process, and improve a quality of a wafer back surface (a gloss level, waviness, stain), and to provide a processed semiconductor wafer.

[0014]

[Means for Solving Problem]

To achieve the object, a method for processing a semiconductor wafer according to the present invention is characterized in that, in the method effecting at least a chamfering step, a lapping step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, acid etching is performed after alkali etching at the etching step, and the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step (claim 1)

[0015]

As described above, at the etching step, the alkali etching is first carried out with respect to the lapped wafer to remove a mechanically damaged layer while maintaining a flatness degree after the lapping, and then the acid etching is performed, thereby improving locally deep pits that remain after the alkali etching, surface roughness, and a sharp irregular shape.

[0016]

At this time, when the acid etching is carried out by using the acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water, waviness (surface roughness in cycles of 2 mm or above) is reduced as compared with that obtained by an acid etchant consisting of a hydrofluoric acid, a nitric acid, and an acetic acid, and a pit depth can be also

decreased. Therefore, a polishing stock removal in a polishing process can be reduced, and productivity of the polishing process can be improved. Further, decreasing the polishing stock removal enables suppressing degradation in a flatness degree in the polishing process, thereby further facilitating manufacture of a wafer having a high flatness degree. It is considered that a viscosity of the phosphoric acid becomes a factor, and a mixed acid chemical hardly enters the pits, whereby an etching rate in the pits is lowered as compared with those on other flat surfaces.
[0017]

Furthermore, according to the present invention, there is provided a method for processing a semiconductor wafer, the method effecting at least a chamfering step, a surface grinding step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, wherein the surface grinding step is performed before the etching step, acid etching is performed after alkali etching at the etching step, and the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step (claim 2).
[0018]

Moreover, in this case, in the method for processing a semiconductor wafer, it is preferable that

a lapping step is added to the method for processing the semiconductor wafer, and processing is performed in the order of the lapping step, the surface grinding step, and the etching step (claim 3).

[0019]

As described above, in the present invention, when the conventional lapping step is completely substituted by the surface grinding step or the surface grinding step is effected before the etching step in addition to the lapping step, a large mechanically damaged layer locally produced due to lapping can be considerably reduced, thus suppressing generation of deep pits.

[0020]

Additionally, a wafer shape can be relatively easily controlled at the surface grinding step as compared with the lapping step, and the same shape can be stably obtained. Further, unevenness in thicknesses of wafers can be suppressed.

[0021]

The surface grinding can remove pits which remain even after a lapped wafer is etched. Thus, performing the surface grinding step after the etching step can be considered, but a pattern called a grinding striation remains on a wafer surface in the surface grinding. It was revealed that a polishing stock removal at the polishing step must be increased to eliminate this grinding striation and a flatness degree of the wafer is

thereby degraded. Thus, in the present invention, the surface grinding step is carried out before the etching step. In a processing incorporating the lapping step in particular, it is preferable to carry out the lapping step, the surface grinding step, and the etching step in the mentioned order.

[0022]

It is to be noted that the performing the chamfering step after the surface grinding step is preferable. Further, when the lapping step is present, adding this step before the lapping step is preferable. That is because a lapping slurry is used at the lapping step, but this lapping slurry hardly enters a wafer central portion when the wafer is not chamfered, and a wafer outer peripheral portion sags in some cases. Furthermore, when both the lapping step and the surface grinding step are provided, performing the plurality of (at least two) chamfering steps is more preferable. That is, the chamfering step is not restricted in particular, and providing this step between appropriate steps depending on a purpose can suffice, and the chamfering step may be counterchanged or may be carried out for a plurality of number of times.

[0023]

Moreover, both the wafer front and back surfaces may be ground at the surface grinding step, or the front surface (a polishing target surface side at the

polishing step when one surface alone is subjected to mirror polishing) alone may be subjected to single-side grinding. In particular, when performing the lapping step before the surface grinding step, the single-side grinding for grinding the polishing target surface alone which is polished at the polishing step is preferable. That is because a back surface (an unground surface) of a final mirror finished wafer after the polishing has the same gloss level or roughness as that of a back surface of a conventionally utilized wafer.

[0024]

When determining the final mirror finished wafer as a double-mirror-finished wafer, performing double-side grinding at the surface grinding step is preferable. In this case, the lapping step is not necessarily required. When the lapping step is eliminated, the number of steps can be reduced, and the polishing stock removal can be decreased for both the front and back surfaces of the wafer even at the polishing step, which is preferable. That is, a surface subjected to polishing at the polishing step undergoes surface grinding. However, if a shape of a back surface of a final polished wafer is not specified in particular, a wafer having a high flatness degree can be obtained by performing double-side grinding at the surface grinding step and single-side polishing at the polishing step.

[0025]

Subsequently, at the etching step which is performed after the surface grinding step, a grinding striation produced at the surface grinding step must be removed. This grinding striation is also one type of mechanically damaged layers, and it is considered that a damage of approximately 6 μm is provided. Therefore, when a wafer subjected to surface grinding is alkali-etched, generation of locally deep pits that appear at the time of the alkali etching after the lapping step can be avoided, but the grinding striation portion subjected to surface grinding remains or are emphasized to have a pit-like shape in some cases.

[0026]

Thus, the alkali etching is combined with the acid etching to prevent pits due to such a grinding striation from being produced at the etching step, and the damage is removed while maintaining the flatness degree of the wafer. That is, at the etching step, the alkali etching is first performed, and then the acid etching is carried out. In this manner, at the etching step, the alkali etching is first performed with respect to the wafer subjected to the surface grinding, a mechanically damaged layer is removed while maintaining a flatness degree after surface grinding, and then the acid etching is carried out, whereby the grinding striation, surface roughness, or a shape irregular shape that remains after the alkali etching can be improved while maintaining the

flatness degree. At this time, it is preferable to set an etching removal of the alkali etching to be larger than an etching removal of the acid etching.

[0027]

Further, at this time, when the acid etching is effected by using an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water, waviness can be further reduced to be smaller than that in the acid etching using a conventionally adopted acid etchant consisting of a hydrofluoric acid, a nitric acid, and an acetic acid, and pits due to the grinding striation can be shallowed. Therefore, a polishing stock removal at the subsequent polishing step can be decreased, and the productivity of the polishing step can be improved. Furthermore, decreasing the polishing stock removal enables suppressing degradation in the flatness degree of the wafer at the polishing step, thereby further facilitating manufacture of the wafer having a high flatness degree.

[0028]

Moreover, according to the present invention, there is provided a method for processing a semiconductor wafer, the method effecting at least a flattening step, an etching step, and a mirror polishing step with respect to a semiconductor wafer obtained by slicing a single-crystal rod, wherein the flattening step is performed before the etching step, acid etching is

performed after alkali etching at the etching step, the acid etching is performed with an acid etchant consisting of a hydrofluoric acid, a nitric acid, a phosphoric acid, and water at this step, a back surface polishing step is carried out and then a front surface polishing step is performed at the mirror polishing step after the acid etching (claim 4).

[0029]

As described above, at the mirror polishing step, when the back surface polishing step is performed and then the front surface polishing step is effected after the acid etching, a quality of the wafer back surface (a gloss level, waviness, stain) can be improved. Furthermore, when the back surface polishing step is provided before the front surface polishing, transference of waviness of the back surface onto the wafer front surface can be reduced, a polishing stock removal of the front surface polishing can be decreased, irregularities of a nanotopography can be eliminated, a reduction in flatness degree due to polishing can be suppressed, and a wafer having a high flatness degree can be obtained as advantages. Moreover, since the polishing stock removal can be reduced, the productivity of the polishing step can be considerably improved.

[0030]

In this case, the flattening step can be a lapping step and/or a surface grinding step (claim 5). As

described above, according to the processing method of the present invention, the lapping step and/or the surface grinding step can be adopted as the flattening step, a shape and a flatness degree of the wafer can be maintained at the subsequent etching step and mirror polishing step, and a grinding striation can be efficiently removed, thereby obtaining a wafer having a high flatness degree and improved surface roughness or irregularities by processing.

[0031]

In this case, it is preferable that, at the back surface polishing step, polishing is carried out in such a manner that a gloss level of 35 to 50% can be obtained (claim 6). When polishing is performed to obtain the gloss level of 35 to 50% in this manner, generation of particles or a contact area for an electrostatic chuck or the like that adsorbs wafers does not become a problem.

[0032]

Additionally, it is preferable to perform grinding at the surface grinding step so as to increase a thickness of a wafer outer peripheral portion (claim 7). Although a wafer having a high flatness degree can be processed in the surface grinding, it is preferable to prepare a wafer having an outer peripheral portion which is approximately 0.06 μm thick (in the range of approximately 5 mm with respect to the periphery) with

respect to the polishing stock removal of 1 μm at the time of polishing in order to increase the flatness degree of the polished wafer. That is because a thickness of the peripheral portion of the wafer tends to be reduced at the etching step and the polishing step that are steps following the surface grinding step. At the surface grinding step, such an outer peripheral portion can be controlled to a thick shape, and stable manufacture can be carried out, whereby a wafer having a high flatness degree can be obtained after the polishing. Further, unevenness in thicknesses of wafers can be suppressed.

[0033]

In this case, it is preferable to set an entire etching removal in the etching step to 30 μm or below on both surfaces (claim 8). When the etching removal is set to 30 μm or below on both surfaces in this manner, a wafer having a high flatness degree can be obtained. In particular, outer periphery sag of a wafer due to the etching can be prevented from occurring.

[0034]

Furthermore, according to the present invention, a polishing stock removal in the mirror polishing step can be set to 7 μm or below (claim 9). At the mirror polishing step according to the present invention, since a wafer having small waviness and very shallow pits can be obtained at the etching step, the polishing stock

removal can be set to a very small value, i.e., 7 μm or below, a mirror finished wafer having a high flatness degree can be obtained, and the productivity of the polishing step can be considerably improved. It is to be noted that setting the polishing stock removal to 2 μm or above is preferable in order to obtain an excellent polished surface.

[0035]

In the etching according to the present invention, as a composition ratio when blending the acid etchant, a hydrofluoric acid concentration is preferably 5 to 15 weigh% and a phosphoric acid concentration is preferably 10 to 40 weight% (claim 10). To decrease a depth of each pit produced by the lapping or the alkali etching after grinding for a reduction in the polishing stock removal, it is preferable for the hydrofluoric acid concentration to be 5 to 15 weight% or below and for the phosphoric acid concentration to be in the range of 10 to 40 weight% at the time of blending the acid etchant (an initial concentration). Under such conditions, a viscosity of the etchant becomes appropriate, an effect for reducing a depth of each pit is high, an influence of a side effect that the phosphoric acid reacts with the hydrofluoric acid is small, and the silicon surface etching can be stably carried out.

[0036]

Moreover, in this case, it is preferable for the

acid etchant to be obtained by dissolving silicon with a concentration of 10 g/L or above (claim 11). When a dissolving amount of silicon is set to be large as described above, a liquid replacement amount can be reduced to restore an original liquid state. As a result, concentration control over the etchant can be facilitated, and the acid etching state can be stabilized. Further, a quality such as waviness can be also improved.

[0037]

In this case, as a composition ratio when using the acid etchant, it is preferable for a hydrofluoric acid concentration to be 1 to 7 weight% and for a phosphoric acid concentration to be 18 to 33 weight% (claim 12). Although the above-described concentration range is preferable as an initial concentration (a concentration at the time of blending), as a composition ratio when actually etching a wafer (a concentration at the time of use), it is preferable for a hydrofluoric acid concentration to be 1 to 7 weight% and for a phosphoric acid concentration to be 18 to 33 weight%. When etching is carried out in this range, a depth of each pit is reduced, and a wafer having an excellent surface state can be obtained. Although the hydrofluoric acid is gradually reduced by repeating the etching treatment, an etching effect becomes too small when the hydrofluoric acid concentration becomes 1 weight% or below. When the

concentration deviates the above-described range, stable processing can be carried out by replacing part or all of a chemical to carry out etching.

[0038]

It is desirable for an alkali etchant of the alkali etching in the present invention to be one of an NaOH aqueous solution and a KOH aqueous solution (claim 13). When such an etchant is provided, an etching treatment effect can be further assuredly exercised, a wafer having a high flatness degree can be obtained, and control over an etching removal can be relatively easily performed, thereby performing adjustment at a low cost.

[0039]

A semiconductor wafer processed by the method according to the present invention (claim 14) is a semiconductor wafer in which etching of deep pit portions intrinsic to an alkali-etched surface is suppressed and surface roughens or a sharp irregular shape is improved, the semiconductor wafer being obtained by performing alkali etching to remove a mechanically damaged layer while maintaining a flatness degree after lapping or grinding and then performing acid etching containing a phosphoric acid. In particular, a pit depth or waviness is improved, and a further flat semiconductor wafer can be provided. Furthermore, a semiconductor wafer having an excellent quality (a gloss level, waviness, stain) of a wafer back

surface can be obtained.

[0040]

Moreover, a semiconductor wafer according to the present invention is a semiconductor wafer (CW) subjected to chemical etching, wherein a maximum value of a pit depth is equal to or below 4 μm, waviness is equal to or below 0.05 μm, and a gloss level is 20 to 70% (claim 15). As described above, according to the present invention, a chemically etched semiconductor wafer having pits with very small depths can be manufactured.

[0041]

Additionally, when the CW is utilized to perform mirror polishing of 7 μm or below, it is possible to provide a semiconductor wafer (PW) having a surface subjected to mirror polishing, wherein SFQRmax is equal to or below 0.1 μm, and the other surface subjected to mirror polishing has a pit depth maximum value of 4 μm or below, waviness of 0.05 μm or below, and a gloss level of 20 to 70% (claim 16). Since the pit depth of the CW can be reduced, a polishing stock removal can be considerably decreased when polishing a surface of this wafer. Although degradation of a flatness degree (especially sag of a wafer peripheral portion) or the like is apt to occur when the polishing stock removal is increased, decreasing the polishing stock removal enables avoiding this occurrence, and a highly flat

wafer having SFQRmax of 0.1 μm or below can be obtained. Further, a gloss level of the wafer back surface can be controlled like a conventional wafer.

[0042]

[Embodiment of the Invention]

Although an embodiment according to the present invention will now be described hereinafter with reference to tables and drawings, the present invention is not restricted thereto.

[0043]

As a result of examining various semiconductor wafer processing methods, especially etching methods for fabricating a chemically-etched wafer having an etched surface where particles or contamination is hardly produced while maintaining a flatness degree after lapping the wafer, the present inventors conceived an idea that alkali etching is first carried out to remove a damage layer while maintaining a flatness degree after lapping, and then acid etching, especially acid etching using a mixed aqueous solution of a hydrofluoric acid, a nitric acid and a phosphoric acid (which may be referred to as a phosphoric acid based mixed acid) as an acid etchant rather than a conventionally adopted mixed aqueous solution of a hydrofluoric acid, a nitric acid and an acetic acid (which may be referred to as an acetic acid based mixed acid) is carried out in order to improve remaining deep pits, surface roughness or

waviness, and they ascertained processing conditions to bring the present invention to completion.

[0044]

First, as basic processing conditions of alkali etching, a wafer having a diameter of 8 inches (200 mm) can be lapped by using lapping abrasive grains of #1200, and it is then subjected to alkali etching using an NaOH aqueous solution having a concentration of 50% at 85°C. Further, as an etching removal of the alkali etching, 10 to 30 μm for both surfaces is an appropriate range. In particular, as conditions that a depth of each locally deep pit is close to a minimum value and TTV and Ra are not seriously degraded, approximately 20 μm is preferable.

[0045]

Here, the locally deep pit means a pit having a size or a depth increased by the alkali etching, the pit being formed when the lapping abrasive grains stick into a wafer surface at the time of lapping. Therefore, the locally deep pit slightly affects the size number of the lapping abrasive grains utilized for the lapping. Furthermore, the pit depth tends to increase when an alkali concentration is low and, on the other hand, the pit depth can be reduced when the alkali concentration is high, but an etching removal must be increase to reduce the pit depth, thereby degrading the efficiency. Moreover, although this pit depth can be obtained based

on a focal depth of an optical microscope, polishing must be carried out at a mirror polishing step as a subsequent step in order to remove the pit. Therefore, a mirror polishing amount must be set to a maximum value or a higher value of such a large pit depth, and hence reducing the pit depth as much as possible is desirable. [0046]

Here, TTV [Total Thickness Variation] (μm) means a numeric value representing a difference in thickness between a thickest portion and a thinnest portion in one wafer, and it is an index of wafer flatness. Additionally, Ra (μm) means central line average roughness, and it is one type of the most frequently utilized surface roughness parameters.
[0047]

Subsequently, a composition of the acid etchant was examined and checked. A phosphoric acid based mixed acid consisting of a hydrofluoric acid, a nitric acid and a phosphoric acid was checked in place of a conventionally utilized acetic acid based mixed acid consisting of a hydrofluoric acid, a nitric acid and an acetic acid. That is, the acid etchant mainly contains the hydrofluoric acid and the nitric acid that can improve surface roughness, and the phosphoric acid is used in placed of the acetic acid which is usually adopted as a liquid added to the above acids. That is because the present inventors considered that the

phosphoric acid is stable among strong acids and an influence of a viscosity of the phosphoric acid enables lowering an etching rate in each pit as compared with that on any other flat surface by interrupting supply of the new liquid after entering each pit, and this tendency was able to be qualitatively grasped.

[0048]

Thus, a mixing ratio of the hydrofluoric acid, the nitric acid and the phosphoric acid was examined. Table 1 shows an acid mixing ratio, a locally deep pit depth of a wafer subjected to the acid etching, and a surface state observation result when a wafer (which may be referred to as a processed wafer hereinafter) subjected to alkali etching of 20 μm on both surfaces after lapping of 60 μm for both the surfaces by using lapping abrasive grains #1200 for improvement in flatness degree of the wafer having a diameter of 8 inches and removal of a mechanically damaged layer is acid-etched by using a mixed acid aqueous solution consisting of the hydrofluoric acid, the nitric acid, the phosphoric acid and the water. Test numbers 1 to 13 represent examples where the mixing ratio of the hydrofluoric acid, the nitric acid and the phosphoric acid is changed, and test numbers 14 and 15 represent examples of a conventional mixed aqueous solution consisting of the hydrofluoric acid, the nitric acid and the acetic acid. 11 g/L of silicon was dissolved in these types of etchants to

stabilize the etchants, then the processed wafer was subjected to etching of 10 μm for both the surfaces, and a pit depth and a surface state were evaluated.

[0049]

[Table 1]

Test number	Mixing ratio (capacity ratio)				(Initial) concentration at mixing (weight%)					Evaluation Item	
	HF	HNO_3	H_3PO_4	CH_3COOH	HF	HNO_3	H_3PO_4	CH_3COOH	H_2O	Pit depth (μm)	Surface state
	50 weight%	70 weight%	85 weight%	100 weight%							
1	1	4	4	-	4.3	29.4	42.1	-	24.2	3.0 (Note 1)	#1
2	1	3	3	-	5.5	28.6	40.9	-	25.0	3.0 (Note 1)	#2
3	1	3	2	-	6.6	34.1	32.5	-	26.8	3.0	#3
4	2	6	3	-	7.3	37.6	26.9	-	28.2	4.4	#3
5	1	2	2	-	7.9	27.0	38.9	-	26.2	3.2	#3
6	1	3	1	-	8.1	42.1	20.1	-	29.7	4.2	#3
7	3	6	2	-	11.3	38.9	18.6	-	31.2	4.0	#3
8	1	1	1	-	13.6	23.4	33.5	-	29.5	3.1	#2
9	2	1	2	-	16.3	14.1	40.2	-	29.4	5.4 (Note 2)	#1
10	2	2	1	-	16.9	29.2	20.9	-	33.0	4.3	#1
11	3	1	3	-	17.5	10.1	43.1	-	29.3	5.8 (Note 2)	#1
12	4	1	4	-	18.1	7.8	44.7	-	29.4	5.6 (Note 2)	#1
13	4	4	1	-	19.3	33.2	11.9	-	35.6	5.2	#1
14	1	2	-	1	11.5	39.4	-	20.8	28.3	7.4	#3
15	1	3	-	2	7.7	39.7	-	27.9	24.7	7.1	#3

(Note 1): Etching is hardly carried out (an etching rate is low).

(Note 2): A pit depth cannot be accurately evaluated because of surface roughness.

Surface state: #3: Excellent

#2: Good

#1: Slightly bad

[0050]

It can be understood from this test result that the pit depth can be greatly improved by changing the acetic acid to the phosphoric acid, and the pit depth is approximately 7 μm when the acetic acid is used, but the pit depth is approximately 3 to 4 μm when the acetic acid is changed to the phosphoric acid. Further, it can be considered that the pit becomes small as a phosphoric acid concentration (weight%) increases.

[0051]

As described that, it can be understood that the effect of the phosphoric acid is large with respect to the pit depth. In regard to the surface state, when the hydrofluoric acid concentration (weight%) is higher than the nitric acid concentration like the test numbers 9, 11 and 12, the surface becomes rough to get smoked, and a gloss level is reduced. When the hydrofluoric acid concentration is too high or the nitric acid concentration is too low, the surface state is degraded. Therefore, it is preferable to perform etching in a state that the hydrofluoric acid concentration is lower than that of the nitric acid. Furthermore, when the hydrofluoric acid concentration is far lower than the nitric acid concentration like the test number 1, etching is not performed (almost no reaction).

Therefore, setting a (hydrofluoric acid/nitric acid) ratio to 1/7 or above is preferable. In a state where etching is hardly carried out (almost no reaction), a wafer surface is in an original alkali-etched surface state, and each deep pit and a rough surface state remain. Moreover, if etching is continued, each pit is reduced in size, but an etching time becomes long, which results in an operational problem. Additionally, an etching rate may be low even though the phosphoric acid concentration is 40 weight% or above. It can be considered that etching does not advance due to an influence of a side effect of the like of the hydrofluoric acid and the phosphoric acid.

[0052]

Taking these matters into consideration, a wafer having a very excellent surface state can be obtained when the (hydrofluoric acid/nitric acid) ratio is approximately 1/2 and the phosphoric acid concentration is 40 weight% or below in particular. A gloss level can be extensively adjusted to 20 to 70% by adjusting an etching time.

[0053]

Here, each surface state in Table 1 is a state that the surface becomes rough and the gloss level is lowered or a state the surface state of the alkali etching remains after conducting a visual appearance inspection, and a surface state that is hardly utilized as it is was

determined as #1 (slightly bad). When the surface state of the alkali etching remains, the surface state can be improved by prolonging the etching time, but there is an operational problem. Further, since the pit depth is small even though the surface is rough, the wafer can be used as a raw material wafer when polishing both surfaces of the wafer. A surface state that the surface is etched with an excellent gloss level but a slight patchy pattern remains was determined as #2 (good). The wafers in these surface states can be utilized without problem. Furthermore, a surface state that has an improved gloss level equivalent to that obtained by the conventional acetic acid based mixed acid and can be adjusted to a gloss level range desired as a product was determined as #3 (excellent). Moreover, the pit depth is a value obtained based on a focal depth of an optical microscope at a portion having a pit after scanning each wafer surface, and it represents a maximum value of the obtained pit depth.

[0054]

Based on the pit depth and the surface state, as an initial concentration at the time of blending, a preferable phosphoric acid based mixed acid concentration range is 5 to 15 weight% for the hydrofluoric acid (HF), 20 to 45 weight% for the nitric acid (HNO_3), 10 to 40 weight% for the phosphoric acid (H_3PO_4), and the remainder for water (H_2O).

[0055]

As to this range, when the hydrofluoric acid concentration at the time of blending is set to 5 weight% or below, an etching effect (responsiveness) is degraded. Additionally, when this concentration is 15 weight% or above, the surface state is degraded because of a relationship between the hydrofluoric acid and the nitric acid. In regard to the nitric acid, a clear finding cannot be obtained in particular, but it can be considered that the range of 20 to 45 weight% is preferable based on a relationship between the nitric acid, the hydrofluoric acid and the phosphoric acid. In particular, 1/(2 to 7) is preferable as the (HF/HNO_3) ratio. As to the phosphoric acid, the pit improving effect is reduced when the concentration is 10 weight% or below, and a side effect with the hydrofluoric acid or wafer is increased, etching becomes unstable, the etching effect is eliminated, and the surface state is degraded when the concentration is 40 weight% or above.

[0056]

As an etching removal of the acid etching, 5 to 20 μm for both surfaces is an appropriate range. In particular, approximately 10 μm for both surfaces enables reducing the pit depth and smoothly etching the surface while maintaining a flatness degree. It can be considered that the mixed acid hardly enters a pit caused due to lapping or a pit at a grinding striation

portion because of an influence of a viscosity of the phosphoric acid, and an etching rate in the pit is lowered as compared with that on any other flat surface.
[0057]

Next, each composition ratio during actual etching was confirmed. At the time of blending, the above-described concentration range is preferable, but the composition actually varies during the etching. When a silicon wafer is etched, in regard to each composition in a chemical, there is a tendency that the hydrofluoric acid concentration is reduced, the nitric acid concentration is gradually decreased, the phosphoric acid concentration hardly varies, and the water concentration is increased. In particular, the composition is unstable immediately after start of the etching.
[0058]

Thus, dissolving silicon in the mixed acid in advance is preferable in order to stabilize the etchant. A composition when dissolving this silicon (a composition at the time of actual use) was confirmed. Table 2 shows each component concentration in the etchant when a silicon dissolving amount is changed from 0 to 20 g/L. A phosphoric acid based mixed acid obtained by mixing 50 weight% of the hydrofluoric acid, 70 weight% of the nitric acid and 85 weight% of the phosphoric acid at a capacity ratio of 1:3:2 as etchant

compositions at the time of blending (an initial stage) equal to those of the test number 13 was utilized, and how the actual etching compositions vary when dissolving this mixed acid in silicon was confirmed.

[0059]

Moreover, since it was confirmed that waviness or peripheral sag can be greatly improved depending on the silicon dissolving amount, each etchant shown in Table 1 was used, lapping was performed with lapping abrasive grains of #1200, and a wafer subjected to alkali etching of 20 μm for both surfaces underwent acid etching of 10 μm for both surfaces to evaluate waviness. Table 2 also shows this result.

[0060]

[Table 2]

	Silicon dissolving amount (g/L)	Etchant composition after dissolving silicon					Waviness (μm)
		HF (weight%)	HNO_3 (weight%)	H_3PO_4 (weight%)	H_2O (weight%)	Other by-product such as H_3SiF_6	
1	0	6.6	34.1	32.5	26.9	-	0.104
2	5	5.3	32.8	32.7	27.6	1.6	0.065
3	10	4.0	31.6	32.9	28.3	3.2	0.044
4	15	2.6	30.2	33.1	29.1	5.0	0.034
5	20	1.2	29.0	32.6	30.6	6.6	0.029

[0061]

As can be seen from Table 2, the concentration at the time of blending (an initial concentration) varies by dissolving silicon in advance. In case of the phosphoric acid based mixed acid obtained by blending 50 weight% of the hydrofluoric acid, 70 weight% of the

nitric acid and 85 weight% of the phosphoric acid at the capacity ratio of 1:3:2, the hydrofluoric acid concentration is approximately 1 to 7 weight%, the nitric acid concentration is 25 to 33 weight%, and the phosphoric acid concentration is 18 to 33 weight% as the etching composition at the time of use, and using these materials in such a composition range is preferable. Further, when the silicon dissolving amount is set to 10 g/L or below, a very excellent wafer having waviness of 0.05 μm or below can be manufactured, which is more preferable. The waviness can be reduced as the silicon dissolving amount is increased.

[0062]

Here, as to the waviness, a height of a measurement start point and a height of a measurement end point are brought in line to provide a height origin, absolute values Y_1 to Y_{29} of a displacement amount from the origin are measured at a pitch of 2 mm, and an average value Y of these values is determined as the waviness. As a waviness measurement device, a universal profilometer (SE-3F type) manufactured by Kosaka Laboratory Ltd. was used. In regard to a measurement method, 60 mm at a central portion on a surface of a wafer (a diameter: 200 mm) was traced by using a sensing pin to measure a shape component alone excluding fine surface roughness components.

[0063]

Furthermore, when 10 g/L or above of silicon is dissolved, the etching component is stabilized. The responsiveness of the etchant immediately after blending is unstable. When a certain amount of silicon is dissolved in advance, the responsiveness and the composition of the etchant are stabilized. Moreover, although almost a full amount of the etchant must be replaced to restore the etching composition to the concentrations immediately after blending before dissolving silicon, restoring the etching component to the state after dissolving silicon is easy, and just partially replacing (adding) the etchant having no silicon dissolved therein can suffice, thereby reducing a liquid replacing amount. As a result, a concentration and unevenness of the etchant can be reduced, control can be facilitated, and the acid etching state can be stabilized.

[0064]

As described above, using the mixed acid containing the phosphoric acid for the acid etching is superior to the conventional acetic acid based mixed acid etching in the following points. That is,

1) a pit depth can be reduced to be smaller than that in the conventional alkali etching + acetic acid based mixed acid etching;

2) a smoothing efficiency is high;

3) the number of waviness components is small; and

4) surface roughness becomes fine, and a gloss level increases.

[0065]

Relationships between various etching methods and qualities and characteristics of obtained wafers are collectively compared in Table 3. It is to be noted that, when etching is performed by using the phosphoric acid based acid aqueous solution and an etching removal is increased, a flatness degree tends to degrade like an example where etching is carried out by using an acetic acid based acid aqueous solution alone. Furthermore, an etching rate is low, and the productivity is poor. When a treatment is carried out by using the (alkali + phosphoric acid based) etchant like the present invention, the etching removal when performing the treatment by using the phosphoric acid based etchant can be reduced, the above-described problem can be improved, and a polishing stock removal at a polishing step can be considerably decreased, which is preferable. Based on the above description, the superiority of the present invention is clear.

[0066]

[Table 3]

Wafer quality / Etchant type	Flatness degree	Waviness	PW polishing stock removal	Back surface state
Alkali solution (NOH or KOH)	#3 (good)	#3 (small)	#4 (many)	#4 (rough)
Acid solution (acetic acid base)	#4 (bad)	#4 (large)	#2 (few)	#3 (smooth)

Combination (alkali + acetic aid base)	#2	#2	#1	#1
Present invention (alkali + phosphoric acid base)	#2	#3	#3	#2

[Note] Acetic acid base (hydrofluoric acid + nitric acid + acetic acid), phosphoric acid base (hydrofluoric acid, + nitric acid + phosphoric acid)

[0067]

It is to be noted that, when an etching removal (a removal stock required by etching) is too large, wafer outer peripheral sag is apt to occur due to etching of performing alkali etching and acid etching. Therefore, it is preferable to reduce the stock removal to be smaller than a conventional stock removal, i.e., to approximately 10 to 30 μm for both surfaces at the etching step. More preferably, the etching step is set to 15 μm for both surfaces in the alkali etching and approximately 5 μm for both surfaces in the acid etching.

[0068]

According to the two-stage chemical etching including the alkali etching + the phosphoric acid based mixed acid etching according to the present invention, it is possible to stably manufacture a semiconductor wafer having a pit depth maximum value of 4 μm or below, a waviness PV value at the 2-mm pitch of 0.05 μm or below, and a gloss level range of 20 to 70%.

[0069]

Further, as a result of examining a method for manufacturing a wafer having less mechanical damages and stay of pits and others due to such damages before the mirror polishing step, especially examining the etching step or its previous step in many ways, the present inventors conceived an idea that a wafer that has less damaged layers produced due to slicing or lapping and maintains a high flatness degree can be obtained by incorporating the surface grinding step in place of the lapping step or after the lapping step and that the alkali etching is performed to remove the damaged layers and grinding striations which remain from the surface grinding and the acid etching is carried out by using a mixed aqueous solution consisting of a hydrofluoric acid, a nitric acid and a phosphoric acid as an acid etchant in order to improve pits generated due to the remaining grinding striations, and they ascertained processing conditions to bring the present invention to completion.

[0070]

FIG. 1 is a series of flowcharts for manufacturing a semiconductor mirror finished wafer by processing a single-crystal rod according to the present invention. FIG. 1(a) is a flowchart sequentially including the surface grinding step and the etching step, and FIG. 1(b) is a flowchart sequentially including the surface grinding step having the lapping step added thereto as a

previous step and the etching step.

[0071]

FIG. 1(a) shows a mirror finished wafer manufacturing process in which the lapping step is completely substituted by the surface grinding step, a single-crystal rod is sliced at a slicing step to obtain a wafer, and the wafer is subjected to surface grinding at the surface grinding step, thereby improving a flatness degree and removing mechanically damaged layers produced at the slicing step. Then, the wafer is chamfered at the chamfering step and enters the etching step. As the etching, alkali etching is first carried out to remove or shallow a damaged layer or a grinding striation, and acid etching is then performed by using a phosphoric acid based mixed acid to shallow the grinding striation. At this time, increasing an etching removal of the alkali etching beyond an etching removal of the acid etching is preferable. Subsequently, mirror polishing is effected at the mirror polishing step, and cleaning/drying is performed at the cleaning/drying step, thereby fabricating a mirror finished wafer having a high flatness degree.

[0072]

FIG. 1(b) shows a mirror finished wafer manufacturing process in which the lapping step is added before the surface grinding step, a single-crystal rod is sliced at the slicing step to obtain a wafer, the

wafer is subjected to coarse chamfering at a primary chamfering step, and then it is lapped at the lapping step to improve a flatness degree and remove a mechanically damaged layer produced at the slicing step. Subsequently, surface grinding is carried out at the surface grinding step to further improve the flatness degree. Then, finish chamfering processing is performed at a secondary chamfering step, and the processing advances to the etching step. As the etching, alkali etching is first performed to remove a damaged layer or a grinding striation, and then acid etching is performed with a phosphoric acid based mixed acid to shallow the grinding striation. At this time, increasing an etching removal of the alkali etching beyond an etching removal of the acid etching is preferable. Subsequently, mirror polishing is carried out at the mirror polishing step, and cleaning/drying is effected at the cleaning/drying step, thereby fabricating a mirror finished wafer having a high flatness degree.

[0073]

First, as standard conditions for the surface grinding, the number of revolutions of a spindle: 4000 to 7000 rpm, the number of revolutions of a wafer: 5 to 9 rpm (processing) or 3 to 7 rpm (spark out), and a grinding stone feed speed: 0.1 to 0.3 μm/sec are preferable. A grinding stone having a high Young's modulus is good as the grinding stone to be utilized,

and an infeed type surface grinding machine having a center cut type grinding stone is preferable as the surface grinding machine. As the surface grinding machine, there is a double-ended grinding machine that simultaneously grinds both surfaces or a machine that grinds surfaces one by one or a single surface alone, but a conformation of the machine is not restricted in particular. To improve the flatness degree and remove a mechanically damaged layer generated due to slicing, performing grinding for 40 to 60 μm with respect to both surfaces (20 to 30 μm with respect to one surface) can generally suffice.

[0074]

Here, although locally deep damages (pits) are formed due to an influence of the lapping grinding stone at the lapping step, the surface grinding enables performing processing with less such local mechanical damages. However, although depending on conditions for the surface grinding step, a grinding striation remains in the surface grinding. This grinding striation is generated when the imprint of cutting of the grinding stone remains as a stripe pattern on a wafer surface.

[0075]

Thus, the above-described etching is carried out. The alkali etching is first performed to remove a damaged layer or a grinding striation, and then the acid etching is performed with a phosphoric acid based mixed

acid to shallow the grinding striation. Subsequently, mirror polishing is effected at the mirror polishing step, and cleaning/drying is performed at the cleaning/drying step, thereby fabricating a mirror finished wafer having a high flatness degree.

[0076]

In the wafer manufactured by performing processing at the series of steps, pits and others are very shallow or not present at all, and waviness components are very few. Surface roughness is fine, and a gloss level is high. Therefore, a polishing stock removal (a removal stock) at the polishing step can be considerably reduced. The wafer having a high flatness degree can be obtained with the high productivity.

[0077]

On the other hand, at the wafer processing step as described above, a reduction in brightness of a wafer back surface (a gloss level), generation of waviness, stain called blue stain (which may be simply referred to as stain hereinafter) that is apt to be produced in a crystal having a low resistivity may occur. The gloss level of the wafer back surface may be lowered to approximately 15 to 20% depending on conditions for the etching step (e.g., when an etching removal is reduced). Thus, to solve this problem, the present inventors conceived an idea that a back surface polishing step is performed after the acid etching and then front surface

polishing step is effected.

[0078]

An example where back surface polishing is performed according to the present invention will now be described hereinafter. FIG. 2 is a series of flowcharts showing an example of a semiconductor wafer processing method having a back surface polishing step according to the present invention. In addition to the semiconductor wafer processing method depicted in FIG. 1, this method is characterized in that a back surface polishing step is effected before the front surface polishing step for mirror-polishing a wafer front surface.

[0079]

At the slicing step, a conventional method/apparatus can be used. For example, using a wire saw or a slicing device having an inner diameter slicer to perform slicing with less warp is preferable. In particular, slicing is effected so as to suppress warp (warpage) to 10 μm or below.

[0080]

At the chamfering step, conventionally utilized method and apparatus can be adopted. It is preferable to perform beveling processing (chamfering processing) for rounding off an outer peripheral corner to avoid chips or cracks on an earlier stage after slicing and to subsequently effect chamfering processing for mirror-finishing a chamfered portion before the front surface

polishing step. In particular, it is preferable to carry out the chamfering step after the surface grinding step. If the lapping step is present, it is preferable to provide the chamfering step before the lapping step. Of course, the plurality of chamfering steps may be provided. In this scheme, the example where the primary chamfering step is provided before the lapping, the secondary chamfering step is provided after the surface grinding, and the mirror chamfering step is provided after the back surface polishing has been explained.

[0081]

At the flattening step, the lapping step alone or the surface grinding step alone may be provided, but the surface grinding step is more preferable since a mechanical damage becomes small, a wafer shape can be relatively easily controlled and the same shape can be stably obtained as compared with the lapping step. The surface grinding step may be added after the lapping step, and processing may be carried out in the order of the lapping step, the surface grinding step and the etching step.

[0082]

It is to be noted that deep pits can be removed by the surface grinding. Therefore, it can be considered that the surface grinding step is provided after the etching step and before the polishing step, but a pattern called a grinding striation remains in case of

the surface grinding. Furthermore, a damage of approximately several μm caused due to grinding also remains. Therefore, a polishing stock removal at the polishing step must be increased to remove this grinding striation. Accordingly, in the present invention, the surface grinding step is carried out before the etching step. In particular, it is preferable to perform the process in which the lapping step is left as it is in the order of the lapping step, the surface grinding step, and the etching step. Performing the process in this order enables removing the deep pits caused due to lapping, and the grinding striation due to the surface grinding can be removed or shallowed.

[0083]

As conditions for the flattening step, in case of the lapping step, using lapping abrasive grains of approximately #1200 to #1500 to perform flattening is preferable. As a lapping stock removal (a removal stock required by the lapping), approximately 40 to 60 μm for both surfaces can suffice. It is preferable to perform two-stage lapping for 40 μm on both surfaces by using lapping abrasive grains of #1200 and for 20 μm on both surfaces by using lapping abrasive grains of #1500. As described above, using a lapping slurry containing fine abrasive grains of #1500 on the latter stage is preferable.

[0084]

When effecting the surface grinding after the lapping, using a grinding stone of approximately #1500 to #4000 is preferable. As a grinding stock removal (a removal stock required by the surface grinding), approximately 10 μm for one surface can suffice. A grinding stone having a high Young's modulus is preferable as the grinding stone utilized for the surface grinding, and an infeed type grinding machine having a center cut type grinding stone is desirable as the grinding machine.

[0085]

When the surface grinding is utilized as the flattening step, a grinding striation remains even after, e.g., a grinding step having less damages. It can be considered that the grinding striation is one type of mechanically damaged layers and it has a slight damage. Therefore, when a wafer subjected to the surface grinding is alkali-etched, local pits that appear at the time of alkali etching after the lapping step can be avoided, but the grinding striation obtained by the surface grinding may remain or may be emphasized to have a pit-like shape in some cases.

[0086]

Although the surface grinding may be performed before the polishing to obtain a wafer having a high flatness degree in conventional examples, but this may lead to, e.g., a problem that the grinding striation

remains. In the present invention, even if the surface grinding is performed at a step before the front surface polishing, the etching and the polishing can be effected to remove the grinding striation while maintaining a shape.

[0087]

That is, at the etching step according to the present invention, as described above, the alkali etching is first performed and then the acid etching is carried out at the etching step. Furthermore, when the acid etching using the hydrofluoric acid, the nitric acid, the phosphoric acid and water is carried out, waviness can be reduced, and the grinding striation can be shallowed.

[0088]

The back surface polishing step is conducted after the acid etching and before the front surface polishing step. This polishing can be carried out at any step after the etching (e.g., the polishing may be performed after the front surface polishing step) if a gloss level of the back surface alone is adjusted, but performing this polishing after the acid etching and before the front surface polishing step enables effecting the front surface polishing in a state that waviness components of the wafer back surface generated by the back surface polishing are improved, and hence an influence of, e.g., transference of a back surface shape can be reduced as

much as possible and irregularities on the nanotopography level an be decreased, thereby polishing the front surface while maintaining a highly flat state. Moreover, as a result, not only a gloss level of the wafer back surface can be adjusted, but also removal of blue stain and others are performed, thus manufacturing a wafer having an excellent back surface quality. Setting the gloss level of the back surface to 35 to 50% is preferable. To realize this value, a polishing stock removal (a removal stock required by the polishing) of 0.4 μm or below and 0.05 μm or above is preferable, or a polishing stock removal of approximately 0.1 μm to 0.3 μm is more preferable.

[0089]

The front surface polishing step is not restricted in particular as long as polishing is carried out under conditions that outer peripheral sag due to polishing does not occur. However, when performing the polishing on a plurality of stages in particular, setting a polishing stock removal to 4 μm or below on the entire front surface side is preferable. However, effecting polishing for approximately 1 μm is desirable in order to obtain an excellent mirror finished surface. Suppressing the polishing stock removal in this manner enables manufacturing a wafer having a high flatness degree while maintaining the flatness degree in previous steps.

[0090]

In particular, since a wafer in which waviness is small and a grinding striation (a pit caused due to the grinding striation) is very shallow at the etching step is obtained from the front surface (mirror) polishing step according to the present invention, a polishing stock removal can be reduced as much as possible, thus obtaining a mirror finished wafer having a high flatness degree. Moreover, since the back surface polishing step is provided before the polishing, transference of waviness on the back surface to the wafer front surface can be suppressed from occurring, and a polishing stock removal of the front surface polishing can be further decreased. As a result, irregularities on the nanotopography can be reduced, a reduction in flatness degree due to the polishing can be suppressed, and a wafer having a high flatness degree can be obtained as advantages. Additionally, since the polishing stock removal can be reduced, the productivity of the polishing step can be considerably improved.

[0091]

[Examples]

Examples and comparative examples of the present invention will now be specifically explained hereinafter, but the present invention is not restricted thereto.

(Example 1) As a result of discussion of the above matters, considering a pit depth, a surface state, an

etching rate, stability of an etchant and others, it was revealed that an etchant containing 50 weight% of a hydrofluoric acid: 70 weight% of a nitric acid: 85 weight% of a phosphoric acid = 1:3:2 as a mixing ratio, i.e., an etchant containing HF=6.6 weight%, HNO_3=34.0 weight%, H_3PO_4=32.5 weight%, H_2O (26.9 weight%) as a remainder, and a silicon dissolving amount=19 g/L is preferable. Examples using this acid etchant will now be described hereinafter.

[0092]

A lap wafer (a lapping abrasive grain number: #1200) having a diameter of 200 mm (8 inches) was utilized to perform the following etching treatment. TTV of this lap wafer was approximately 0.8 μm. First, as alkali etching, an etching removal target was set to 20 μm for both surfaces, and the wafer was immersed in an NaOH aqueous solution having a concentration of 50 weight% at 85°C for 450 seconds. Then, the wafer was immersed in a hydrogen peroxide solution of 0.3% as a hydrophilicity treatment, and then acid etching was finally performed with the mixed acid containing 50 weight% of the hydrofluoric acid: 70 weight% of the nitric acid: and 85 weight% of the phosphoric acid = 1:3:2 (a capacity ratio) at a liquid temperature of 25°C with an etching removal target being set to 10 μm for both surfaces. A flatness degree (TTV), surface roughness (Ra), waviness, a pit depth, and a gloss level

of each wafer subjected to the etching were measured to examine an etching effect. Table 4 shows its result.

[0093]

(Comparative Example 1) The etching was performed under the same conditions as those of Example 1 except that a mixed acid containing 50 weight% of the hydrofluoric acid: 70 weight% of the nitric acid: 100 weight% of the acetic acid = 1:2:1 (a capacity ratio) as a conventional acetic acid based mixed acid was used as the etchant. A result of this etching is also shown in Table 4.

[0094]

[Table 4]

Quality of Wafer (CW Wafer) after Alkali Etching and Acid Etching

	Number of processed wafers	TTV (μm)	Ra (μm)	Waviness (μm)	Pit depth (μm)	Gloss level (%)
Example 1	150	0.92	0.16	0.029	3.2	40
Comparative Example 1	50	1.01	0.23	0.034	6.0	36

[0095]

Based on Table 4, wafers each having a very excellent flatness degree (TTV) or waviness were obtained in Example 1 (the phosphoric acid based mixed acid). Further, the wafers each having a very small pit depth were manufactured. Each gloss level was a value equal to that in the conventional example, and it can be understood that this value can be adjusted to fall

within a standard range. Furthermore, surface roughness (Ra) of a wafer chamfered portion was also good, and an effect of, e.g., reducing a load for mirror chamfering can be obtained.

[0096]

Subsequently, CW wafer surfaces according to Example 1 and Comparative Example 1 were polished. A polishing removal was set to 7 μm (a target value) on the entire front surface side. As polishing conditions, polishing was carried out by using a polishing device: a single-wafer processing type polishing device, a polishing pad: a nonwoven type polishing pad, and a polishing agent: a colloidal silica polishing agent (pH=10.5).

[0097]

TTV and SFQRmax of each polished product were measured to examine an appearance. Here, SFQR (Site Front least-sQuares Range) means a value obtained by calculating an average surface as a surface reference in accordance with each site in regard to a flatness degree and representing a maximum range of irregularities for this plane, and SFQRmax represents a maximum value in SFQRs in all sites on a wafer. Table 5 shows a result. Further, in Comparative Example 1, polishing was further effected, and it was continued until an appearance defect is no longer observed (Comparative Example 1b).

[0098]

[Table 5]

Quality of Wafer (PW Wafer) after Polishing

	Number of processed wafers	TTV (μm)	SFQRmax (μm)	Appearance	Polishing stock removal (μm)
Example 1	150	0.68	0.095	Normal	6.97
Comparative Example 1	50	0.70	0.125	Pits remain	6.95
Comparative Example 1b	50	0.78	0.161	Normal	9.90

[0099]

Here, the flatness degree TTV and SFQRmax were measured by using a flatness measuring instrument (U/G9500, U/S9600) manufactured by ADE, and the surface roughness (Ra) was measured by using a universal profilometer (SE-3C type) manufactured by Kosaka Laboratory Ltd. Furthermore, the flatness degree SFQRmax was evaluated in an area of 20 mm×20 mm by using the flatness measuring instrument manufactured by ADE. In regard to the appearance, presence/absence of pits was confirmed by using a microscope.

[0100]

As can be understood from the above result, in Example 1, wafers each having a high flatness degree and no appearance defect (a pit) were manufactured by the polishing with the polishing removal of 7 μm or below. This manufacture was achieved by performing the alkali etching and the acid etching using the phosphoric acid

in the mentioned order and reducing a pit depth after the etching to be smaller than that in conventional examples. Further, since the polishing stock removal can be reduced, a polishing efficiency can be improved, and the outer peripheral sag caused due to the polishing can be avoided, thereby manufacturing wafers each having an excellent flatness degree at a wafer outer periphery.
[0101]

As described above, the flatness degree and the pit depth of the CW wafer are improved by performing the alkali etching and the acid etching utilizing the phosphoric acid. Furthermore, the wafer having less waviness can be obtained. The gloss level in each of Comparative Example and Example can be adjusted to approximately the same extent.
[0102]

Each PW wafer has the appearance defect in Comparative Example, and it can be understood that the polishing stock removal is insufficient. Usually, to completely eliminate the pits after the etching, excessive polishing corresponding to a pit depth + approximately 3 μm is required. Increasing a polishing amount results in prolonging a processing time. Moreover, as can be seen from Comparative Example, SFQRmax is degraded when the polishing stock removal increases. The smaller polishing stock removal is preferable. The polishing stock removal can be reduced

in the acid etching using the phosphoric acid, thus manufacturing each mirror finished wafer having an improved flatness degree, e.g., SFQRmax.

[0103]

(Example 2) A mirror finished wafer was fabricated by such a process as depicted in FIG. 1(b). An ingot having a diameter of approximately 200 mm was sliced and subjected to primary chamfering, then a lapping slurry (a lapping abrasive grain number: #1200) was used, and a lapped wafer (which is called a lap wafer) was utilized to perform the surface grinding under the following conditions.

[0104]

An infeed type single-side grinding machine was utilized to perform the surface grinding at 5500 rpm as the number of revolutions of a spindle, 7 rpm as the number of revolutions of the wafer, and 0.2 μm/sec as a grinding stone feed speed. Thereafter, secondary chamfering was effected. A flatness degree (TTV) of the wafer after this surface grinding was approximately 0.6 μm.

[0105]

Subsequently, in regard to the alkali etching, an etching removal target was set to 20 μm for both surfaces, and the wafer was immersed in an NaOH aqueous solution having a concentration of 50 weight% at 85°C for 450 seconds to carry out the etching. Subsequently, as

a hydrophilicity treatment, the wafer was immersed in a hydrogen peroxide solution of 0.3%, and the acid etching was carried out with a mixed acid containing 50 weight% of the hydrofluoric acid: 70 weight% of the nitric acid: 85 weight% of the phosphoric acid = 1:3:2 (a capacity ratio) at a liquid temperature of 25°C with an etching removal target being determined as 10 μm for both surfaces.

[0106]

A flatness degree (TTV), surface roughness (Ra), waviness, appearance inspection (and a pit depth), a gloss level on a wafer back surface of each wafer subjected to the acid etching were measured to examine an effect of the surface grinding and the etching.

[0107]

The TTV was measured by using the flatness measuring instrument (U/G9500, U/S9600) manufactured by ADE, and Ra was measured in regard to a wafer central portion by using the universal profilometer (SE-3C type) manufactured by Kosaka Laboratory Ltd.

[0108]

In regard to the waviness, a height of a measurement start point and a height of a measurement end point are brought in line to provide a height origin, absolute values Y_1 to Y_{29} of a displacement amount from the origin are measured at a pitch of 2 mm, and an average value of these absolute values is defined as the

waviness. As a waviness measuring device, a universal profilometer (SE-3F type) manufactured by Kosaka Laboratory Ltd. was used. In regard to the measurement, 60 mm at a central portion on a surface of the wafer was traced by using a sensing pin to measure a shape component alone excluding fine surface roughness components.

[0109]

As to the appearance inspection, presence/absence of pits was observed by using a microscope. When a pit was observed, a pit depth was confirmed. The pit depth was obtained based on a focal depth of an optical microscope. The pit depth is represented by a maximum value of a plurality of evaluated wafers.

[0110]

The gloss level on the wafer back surface was obtained by a glossmeter manufactured by Toyo Seiki Co., Ltd. Table 6 shows a result of the above-described measurements.

[0111]

[Table 6]

Item Example No.	Number of processed wafers	TTV (μm)	Ra (μm)	Waviness (μm)	Pit depth (μm)	Gloss level (%)
Example 2	28	0.60	0.12	0.051	1.0	35
Comparative Example 2	50	1.01	0.23	0.060	6.0	36

[0112]

Then, each wafer subjected to the etching was mirror-polished. A surface subjected to the surface grinding was first polished, and a polishing stock removal was set to a target value 4 μm. The polishing was carried out by using a polishing machine; a single-wafer processing polishing machine, a polishing pad; a nonwoven type polishing pad, and a polishing agent; a colloidal silica polishing agent (pH=10.5) as polishing conditions.

[0113]

TTV and SFQRmax of each polished wafer were measured, and appearance inspection was conducted. SFQR was measured by using a flatness measuring instrument manufactured by ADE, and a size of a site was evaluated in an area of 20 mm × 20 mm. Table 7 shows a result.

[0114]

[Table 7]

Item Example No.	Number of processed wafers	TTV (μm)	SFQRmax (μm)	Appearance inspection	Polishing stock removal (μm)
Example 2	28	0.71	0.120	Normal	4.00
Comparative Example 2-a	50	0.70	0.125	Pits remain	4.00
Comparative Example 2-b	50	0.78	0.161	Normal	9.90

[0115]

As can be understood from the result, in Example 2,

a wafer having a high flatness degree and no appearance defect (a grinding striation or a pit) was manufactured by the polishing with the polishing stock removal of 4 μm or below. This manufacture was achieved by performing the etching, especially effecting the surface grinding before the alkali etching and carrying out the acid etching using the mixed acid containing the phosphoric acid after the alkali etching at the etching step.

[0116]

(Comparative Example 2) Like Example 2, a lap wafer (a lap abrasive grain number: #1200) having a diameter of 200 mm was utilized to subsequently perform the etching treatment. The etching was effected on two stages, i.e., alkali etching and acid etching using a mixed acid containing a hydrofluoric acid, a nitric acid, and an acetic acid.

[0117]

In regard to the alkali etching, an etching removal target was set to 20 μm for both surfaces, and the wafer was immersed in an NaOH aqueous solution having a concentration of 50 weight% at 85°C for 450 seconds to perform etching. Then, as a hydrophilicity treatment, the wafer was immersed in a hydrogen peroxide solution

of 0.3%, and then the acid etching was carried out at a liquid temperature of 25°C by using a mixed acid containing 50 weight% of the hydrofluoric acid, 70 weight% of the nitric acid, and 100 weight% of the acetic acid = 1:2:1 (a capacity ratio) with an etching removal target being set to 10 μm for both surfaces.

[0118]

A flatness degree (TTV), surface roughness (Ra), waviness, appearance inspection (and a pit depth), and a gloss level of each wafer subjected to the etching were measured. Table 6 also shows a result of these measurements.

[0119]

Then, the wafer subjected to the etching was mirror-polished. A polishing stock removal was set to 4 μm as a target value. Polishing conditions are the same as those of Example 2. TTV and SFQRmax of each polished wafer were measured, and appearance inspection was performed. Table 7 shows a result. As can be understood from the result, pits were present when the polishing stock removal was 4 μm in Comparative Example 2 (Table 7: Comparative Example 2-a).

[0120]

Further, the polishing was continued, and the

polishing was performed until the pits were eliminated (Table 7: Comparative Example 2-b). As a result, the pits were eliminated by polishing the entire front surface side for approximately 10 μm, but a flatness degree was slightly degraded.

[0121]

(Example 3) A mirror finished wafer was manufactured by such a process as depicted in FIG. 2. A single-crystal rod (an ingot) having a diameter of 200 mm and a resistivity of 0.02 Ω·cm was sliced by a wire saw to be subjected to primary chamfering, and then a lapping slurry (a lapping abrasive grain number: #1200) was utilized to perform lapping for 40 μm on both surfaces. Subsequently, the lapping slurry was changed to one having a lapping abrasive grain number #1500, and lapping was carried out for 20 μm on both surfaces.

[0122]

Subsequently, the surface grinding was effected. An infeed type single-side grinding machine was used for the surface grinding, and one surface was ground for 10 μm by using a grinding stone of #4000. The grinding was carried out at 5500 rpm as the number of revolutions of a spindle, 7 rpm as the number of revolutions of a wafer, and 0.2 μm/sec as a grinding stone feed speed as surface

grinding conditions. Then, secondary chamfering was carried out.

[0123]

On this stage, although local damages (pits) were formed due to an influence of the lapping abrasive grains at the time of lapping in the conventional examples, processing was performed based on the surface grinding with less local mechanical damages. A flatness degree (TTV) of the wafer after the surface grinding was approximately 0.6 μm.

[0124]

Then, as the etching step, in alkali etching, an etching removal target value was first set to 15 μm on both surfaces, and the wafer was immersed in an NaOH aqueous solution having a concentration of 50 weight% at 85°C to be etched. Subsequently, as a hydrophilicity treatment, the wafer was immersed in a hydrogen peroxide solution of 0.3%, an etching removal target value was set to 5 μm for both surfaces, and acid etching was performed with a mixed acid containing 50 weight% of the hydrofluoric acid: 70 weight% of the nitric acid: 85 weight% of the phosphoric acid = 1:3:2 (a capacity ratio) at a liquid temperature of 25°C.

[0125]

Then, a wafer back surface was polished. The polishing was carried out with a polishing machine: a single-wafer processing type polishing machine, a polishing pad: a nonwoven type polishing pad, and a polishing agent: a colloidal silica polishing agent (pH=10.5) as polishing conditions. The polishing was effected with a polishing stock removal of 0.1 μm. It is to be noted that this polishing stock removal can be set to approximately 0.05 to 0.3 μm depending on a gloss level.

[0126]

A chamfered portion of a wafer outer peripheral portion was mirror-polished. A surface of the wafer subjected to such a process was mirror-polished. The polishing was carried out on a plurality of stages (three stages, i.e., primary polishing, secondary polishing, and finish polishing). A polishing stock removal on the entire front surface side was set to a target value 3 μm. The polishing was performed with a polishing machine: a single-wafer processing type polishing machine, a polishing pad: a nonwoven type polishing pad, and a polishing agent: a colloidal silicon polishing agent (pH=10.5) as main polishing conditions.

[0127]

TTV, SFQRmax, a back surface gloss level, appearance inspection, and nanotopography of each polished wafer were confirmed.

[0128]

TTV and SFQR were measured by using a flatness measuring instrument (U/G9500, U/S9600) manufactured by ADE. SFQR was measured by using the flatness measuring instrument manufactured by ADE, and a size of a site was evaluated in an area of 20 mm × 20 mm.

[0129]

In regard to the appearance inspection, presence/absence of pits was observed by using a microscope. When a pit was observed, a pit depth was confirmed. The pit depth was obtained based on a focal depth of an optical microscope. Moreover, occurrence of stain or the like on the wafer back surface was visually confirmed.

[0130]

Reference was made to JIS Z 8741 (a specular gloss level measuring method), and a gloss level was measured by using a specular glossmeter (a glossmeter SD) specified by this standard based on a method conforming to this standard.

[0131]

The nanotopography (which is also referred to as nanotopology) means irregularities having a wavelength of approximately 0.1 mm to 20 mm and an amplitude of approximately several nm to 100 nm and, as its evaluation method, a difference in height between irregularities on a wafer surface (a P-V value; peak to valley) is evaluated in a region of a block range (this range is called WINDOW SIZE or the like) having a square shape having each side of approximately 0.1 mm to 10 mm or a circular shape having a diameter of approximately 0.1 mm to 10 mm. This P-V value is also called a Nanotopography Height or the like. As the nanotopography, a smaller maximum value of irregularities which present within an evaluated wafer surface is desired in particular. In this example, a plurality of block ranges each having a square shape of 10 mm were evaluated, and a maximum value of their PV values was evaluated. Table 8 shows a result.

[0132]

[Table 8]

	TTV (μm)	SFQRmax (μm)	Back surface gloss level (%)	Appearance inspection	Nanotopography (nm)

Example 3	0.70	0.118	41	Both front and back surfaces are normal	50.0
Comparative Example 3	0.78	0.160	36	Stain was confirmed on back surface	103.2

[0133]

As can be understood from the result, each wafer having a high flatness degree and no appearance defect (a grinding striation or a pit and blue stain on a back surface) was manufactured by the polishing having the polishing stock removal of 4 μm or below in Example 3. In particular, small irregularities on the nanotopography level were improved, which is obviously preferable.

[0134]

This manufacture was achieved by performing the etching, especially performing the surface grinding before the alkali etching and effecting the etching using the mixed acid containing the phosphoric acid after the alkali etching at the etching step and by polishing the back surface. Further, stain and others were not found on the wafer back surface, and the gloss level was controlled to an appropriate value, which is excellent.

[0135]

(Comparative Example 3) A mirror finished wafer was

manufactured by such a process as depicted in FIG. 3. Like Example 3, a single-crystal rod (an ingot) having a diameter of 200 mm and a resistivity of 0.02 Ω·cm was sliced by using a wire saw to be subjected to primary chamfering, and then a lapping slurry (a lapping abrasive grain number: #1200) was utilized to effect lapping for 40 μm on both surfaces. Subsequently, the lapping slurry was changed to a counterpart having a lapping abrasive grain number #1500 to further carry out lapping for 20 μm on both the surfaces.

[0136]

Then, an etching treatment was performed. The etching was effected on two stages, i.e., alkali etching and acid etching using a mixed acid containing a hydrofluoric acid, a nitric acid and an acetic acid. As the alkali etching, an etching removal target value was set to 20 μm for both surfaces, and the wafer was immersed in an NaOH aqueous solution having a concentration of 50 weight% at 85°C for 450 seconds to be etched. Subsequently, as a hydrophilicity treatment, the wafer was immersed in a hydrogen peroxide solution of 0.3%, and an etching removal target value was set to 10 μm for both the surfaces to carry out the acid etching at a liquid temperature of 25°C with a mixed acid containing 50 weight% of the hydrofluoric acid: 70 weight% of the nitric acid: 100 weight% of the acetic acid = 1:2:1 (a capacity ratio).

[0137]

A surface of the wafer subjected to such a process was mirror-polished like Example 3. The polishing was carried out on a plurality of stages (three stages, i.e., primary polishing, secondary polishing, and finish polishing). A polishing stock removal on the entire surface was set to a target value 3 μm. The polishing was performed with a polishing machine: a single-wafer processing type polishing machine, a polishing pad: a nonwoven type polishing pad, and a polishing agent: a colloidal silicon polishing agent (pH=10.5) as main polishing conditions.

[0138]

TTV, SFQRmax, a back surface gloss level, appearance inspection, and nanotopography of each polished wafer were confirmed like Example 3. Table 8 shows a result. As can be understood from the result, each of TTV, SFQRmax and the nanotopography is a value inferior to that of Example 3. Furthermore, stain was observed in this wafer having a small resistivity.

[0139]

It is to be noted that the present invention is not restricted to the foregoing embodiment. The foregoing embodiment is just an example, and any example that has a configuration substantially equal to the technical concept and demonstrates the same functions and effects described in claims of the present invention is included

in the technical scope of the present invention.

[0140]

For example, when a lap wafer having a higher flatness degree than those of the above examples is utilized to be etched, a wafer having a better flatness degree than the above examples can be manufactured. That is, although degradation in the flatness degree due to the etching can be reduced in the present invention, an absolute value of TTV is also affected by a quality of the lap wafer.

[0141]

Moreover, a pit depth is also slightly affected by the number of the lapping abrasive grains used for the lapping. Usually, the lapping abrasive grains of approximately #1200 are used in the lapping step, but utilizing the lapping abrasive grains of #1500 enables further improving the pit depth.

[0142]

Additionally, in this example, as conditions for obtaining a wafer having a high flatness degree, the alkali etching is performed for approximately 20 μm on both surfaces and the acid etching is carried out with an etching removal of approximately 10 μm on both surfaces, but the etching removal is not restricted thereto, and a percentage of the alkali etching may be lowered depending on, e.g., a wafer state after the lapping, or the entire etching removal may be further

reduced. When percentages of the alkali etching and the acid etching are adjusted depending on a demanded wafer quality, a wafer having a high flatness degree and a small pit depth can be manufactured.

[0143]

Additionally, for example, in this example, the manufacture of the wafer subjected to sophisticated single-side mirror finishing alone has been explained, but the present invention is not restricted thereto, and it can be adapted to the manufacture of a wafer having both surfaces subjected to sophisticated mirror finishing. In a CW obtained by the alkali etching and the acid etching containing the phosphoric acid, since a pit depth is improved on both front and back surfaces, a polishing stock removal can be reduced even in case of polishing both the surfaces, thereby obtaining a wafer having a high flatness degree by processing like the single-side mirror finishing.

[0144]

In particular, it is preferable to perform such a process in which such a lapping step is eliminated as depicted in FIG. 1(a), and both the surfaces can be ground by using a double-ended grinding machine at the surface grinding step. Then, since the pit depth is improved on both the front and back surfaces of the wafer subjected to the alkali etching and the acid etching containing the hydrofluoric acid, and the

polishing stock removal can be reduced even when polishing both the surfaces, thereby obtaining a wafer having a high flatness degree from processing like the single-side polishing.

[0145]

Further, for example, although the example where the silicon wafer having a diameter of 200 mm (8 inches) is manufactured has been explained in the foregoing embodiment, the present invention is not restricted thereto, and it can be also applied to a silicon single crystal having a diameter of 4 to 16 inches or above.

[0146]

[Effect of the Invention]

As described above, according to the present invention, when the phosphoric acid based mixed acid is used after the alkali etching, etching of a deep pit portion which is intrinsic to an alkali-etched surface can be suppressed by a high viscosity effect demonstrated by addition of the phosphoric acid, a smooth surface can be obtained, a mirror polishing stock removal can be decreased, and the productivity of the polishing step can be improved. Furthermore, waviness can be improved, and a flatness degree after the mirror polishing can be increased. Moreover, since a stock removal in the mirror polishing can be reduced, and a flatness degree in the polishing step can be suppressed, thereby readily manufacturing a wafer having a high

flatness degree.

[0147]

Additionally, a chemical etching wafer having a smooth irregular shape in which a mechanically damaged layer is removed while maintaining a wafer flatness degree, surface roughness is improved and a depth of a generated pit can be reduced in particular can be fabricated, and the method for manufacturing a semiconductor wafer by which a polishing stock removal in the mirror polishing step is reduced to approximately 4 μm on the entire surface and the semiconductor wafer can be provided. Therefore, the productivity of the mirror polishing and the wafer flatness degree can be improved, and a reduction in cost of the mirror polishing step and an improvement in equality can be achieved. Further, a gloss level on a wafer back surface or contamination on a surface called blue stain can be avoided.

[Brief Description of Drawings]

[FIG. 1] FIG. 1 is flowcharts showing a process for processing and manufacturing a semiconductor mirror finished wafer from a single-crystal rod, wherein (a) is a flowchart showing an example of a manufacturing process according to the present invention, and (b) is a flowchart showing another manufacturing process according to the present invention.

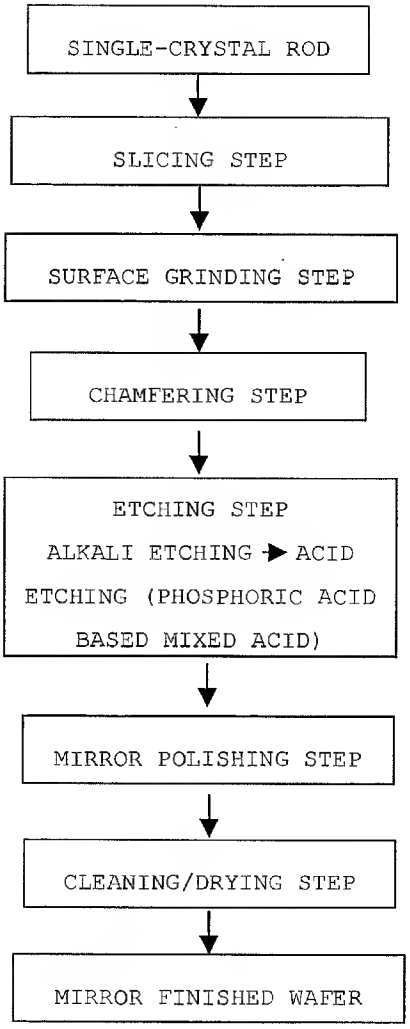
[FIG. 2] FIG. 2 is a flowchart showing a method for

processing a semiconductor wafer having a back surface polishing step according to the present invention.

[FIG. 3] FIG. 3 is a flowchart showing an example of a conventional manufacturing process.

Fig. 1

(a)


SINGLE-CRYSTAL ROD
SLICING STEP
SURFACE GRINDING STEP
CHAMFERING STEP
ETCHING STEP
ALKALI ETCHING → ACID ETCHING (PHOSPHORIC ACID BASED MIXED ACID)
MIRROR POLISHING STEP
CLEANING/DRYING STEP
MIRROR FINISHED WAFER

(b)

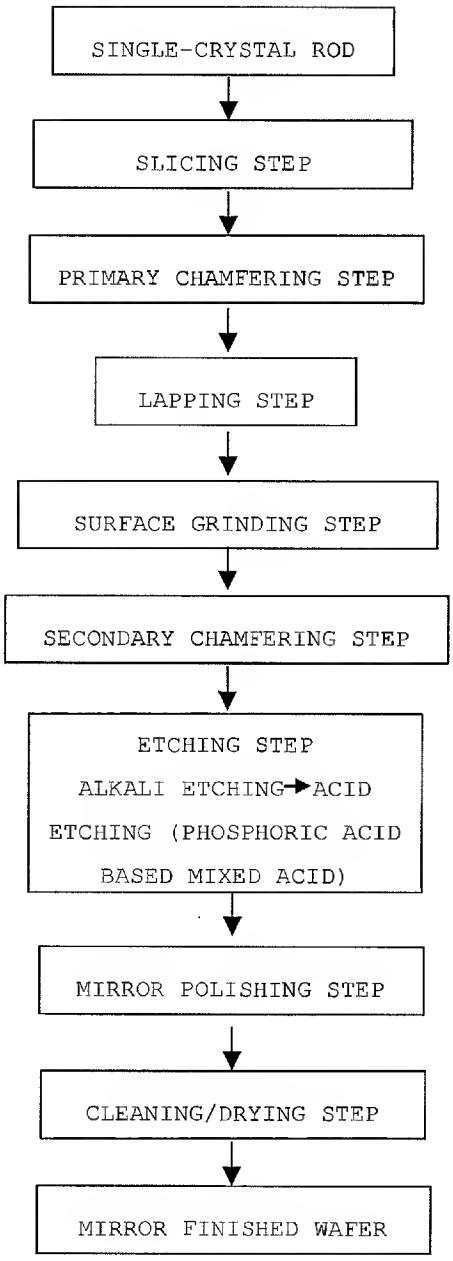

SINGLE-CRYSTAL ROD
SLICING STEP
PRIMARY CHAMFERING STEP
LAPPING STEP
SURFACE GRINDING STEP
SECONDARY CHAMFERING STEP
ETCHING STEP
ALKALI ETCHING → ACID ETCHING (PHOSPHORIC ACID BASED MIXED ACID)
MIRROR POLISHING STEP
CLEANING/DRYING STEP
MIRROR FINISHED WAFER

Fig. 2

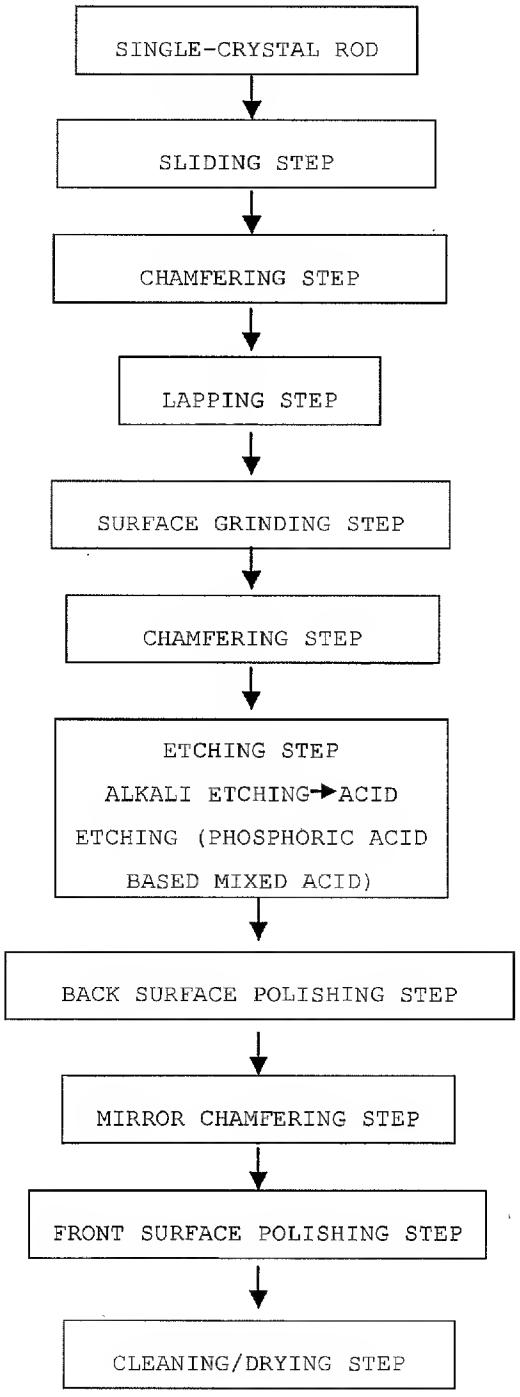
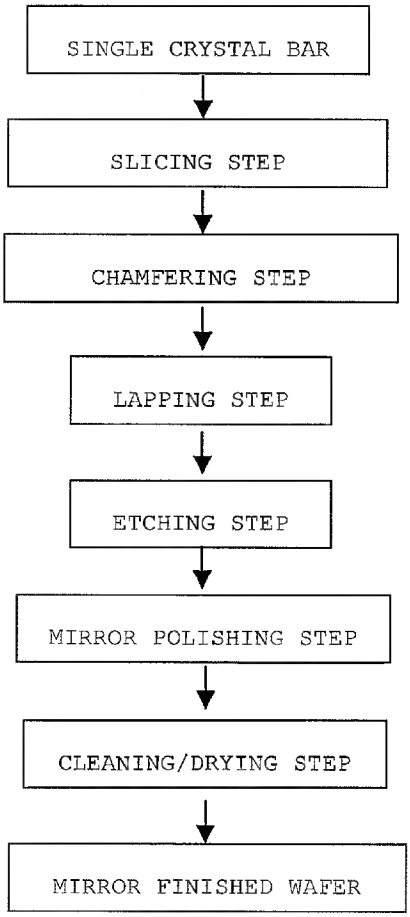

SINGLE-CRYSTAL ROD
SLIDING STEP
CHAMFERING STEP
LAPPING STEP
SURFACE GRINDING STEP
CHAMFERING STEP
ETCHING STEP
ALKALI ETCHING→ACID
ETCHING (PHOSPHORIC ACID
BASED MIXED ACID)
BACK SURFACE POLISHING STEP
MIRROR CHAMFERING STEP
FRONT SURFACE POLISHING STEP
CLEANING/DRYING STEP

Fig. 3


SINGLE CRYSTAL BAR
SLICING STEP
CHAMFERING STEP
LAPPING STEP
ETCHING STEP
MIRROR POLISHING STEP
CLEANING/DRYING STEP
MIRROR FINISHED WAFER